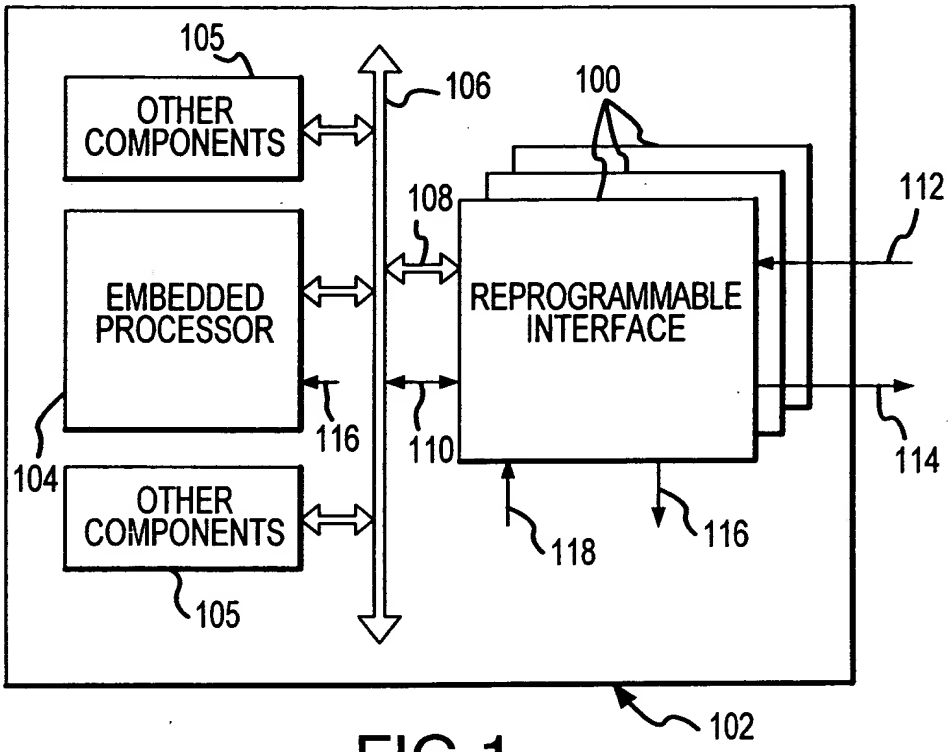
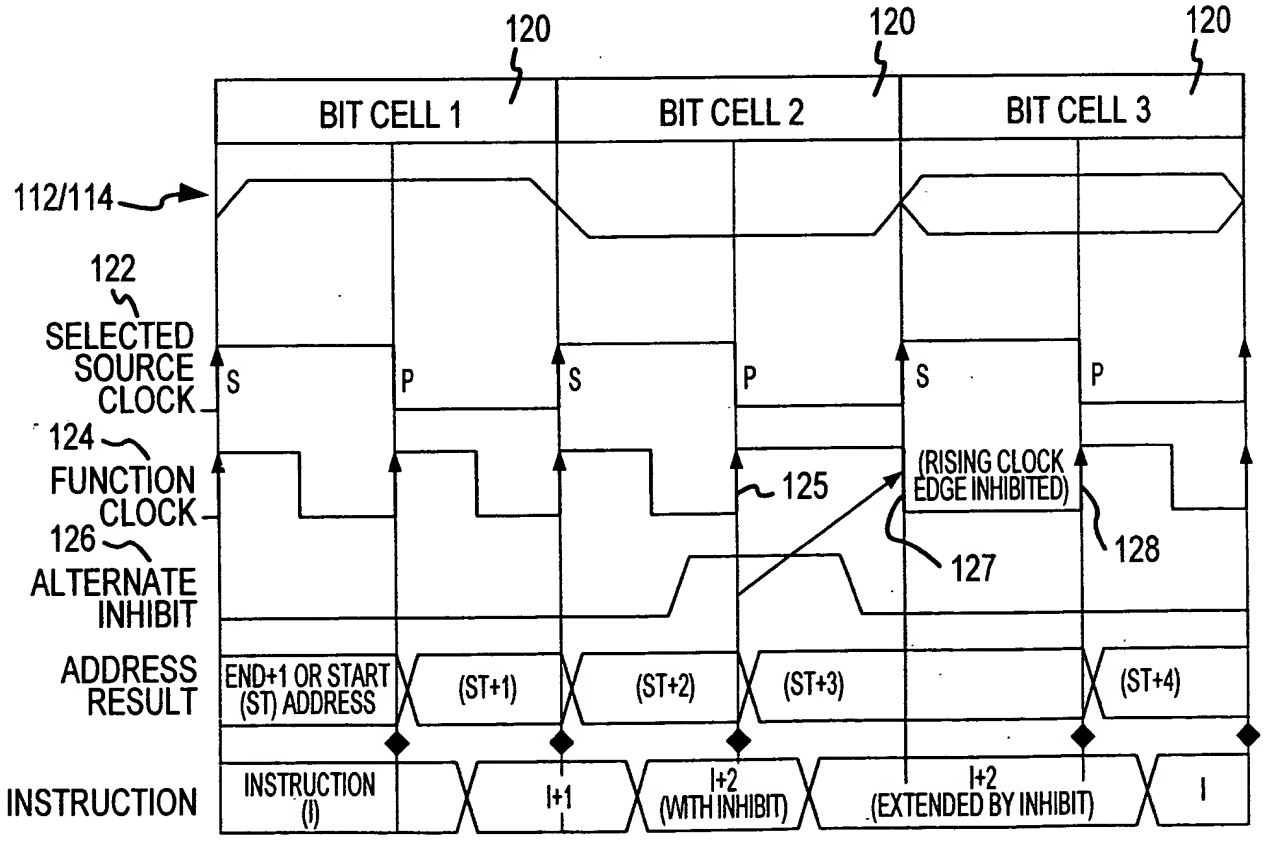

105
OTHER COMPONENTS
106
100
108
112
EMBEDDED PROCESSOR
REPROGRAMMABLE INTERFACE
116
110
114
104
OTHER COMPONENTS
118
116
105
102

FIG.1


120
120
120
BIT CELL 1
BIT CELL 2
BIT CELL 3
112/114
122
SELECTED SOURCE CLOCK
S
P
S
P
S
P
124
FUNCTION CLOCK
125
(RISING CLOCK EDGE INHIBITED)
126
ALTERNATE INHIBIT
127
128
ADDRESS RESULT
END+1 OR START (ST) ADDRESS
(ST+1)
(ST+2)
(ST+3)
(ST+4)
INSTRUCTION
INSTRUCTION (I)
I+1
I+2 (WITH INHIBIT)
I+2 (EXTENDED BY INHIBIT)
I

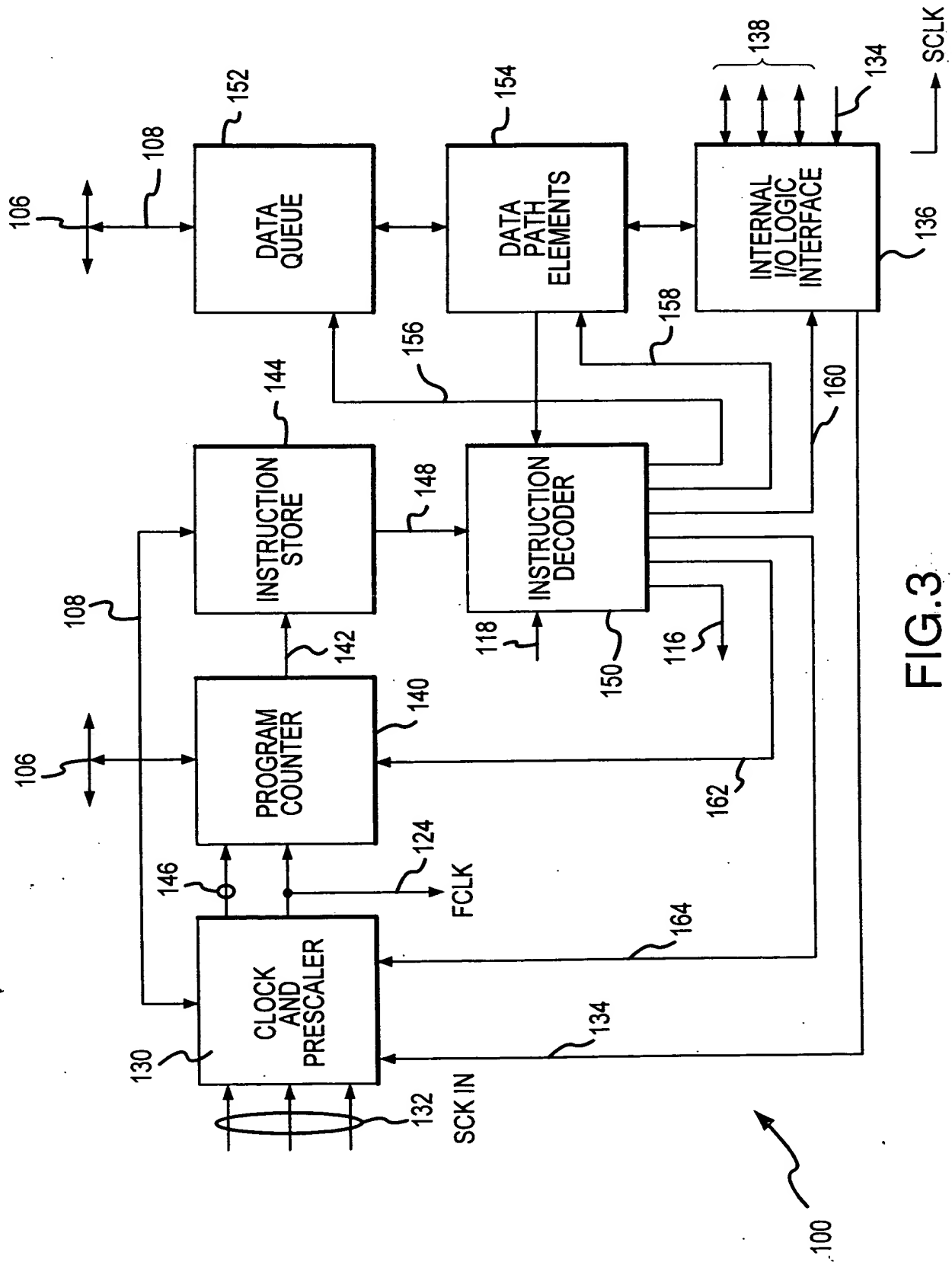

DATA QUEUE
DATA PATH ELEMENTS
INTERNAL I/O LOGIC INTERFACE
INSTRUCTION STORE
INSTRUCTION DECODER
PROGRAM COUNTER
CLOCK AND PRESCALER
SCK IN
FCLK
SCLK
100
106
108
130
132
134
136
138
140
142
144
146
148
150
152
154
156
158
160
162
164
116
118
124

FIG.3

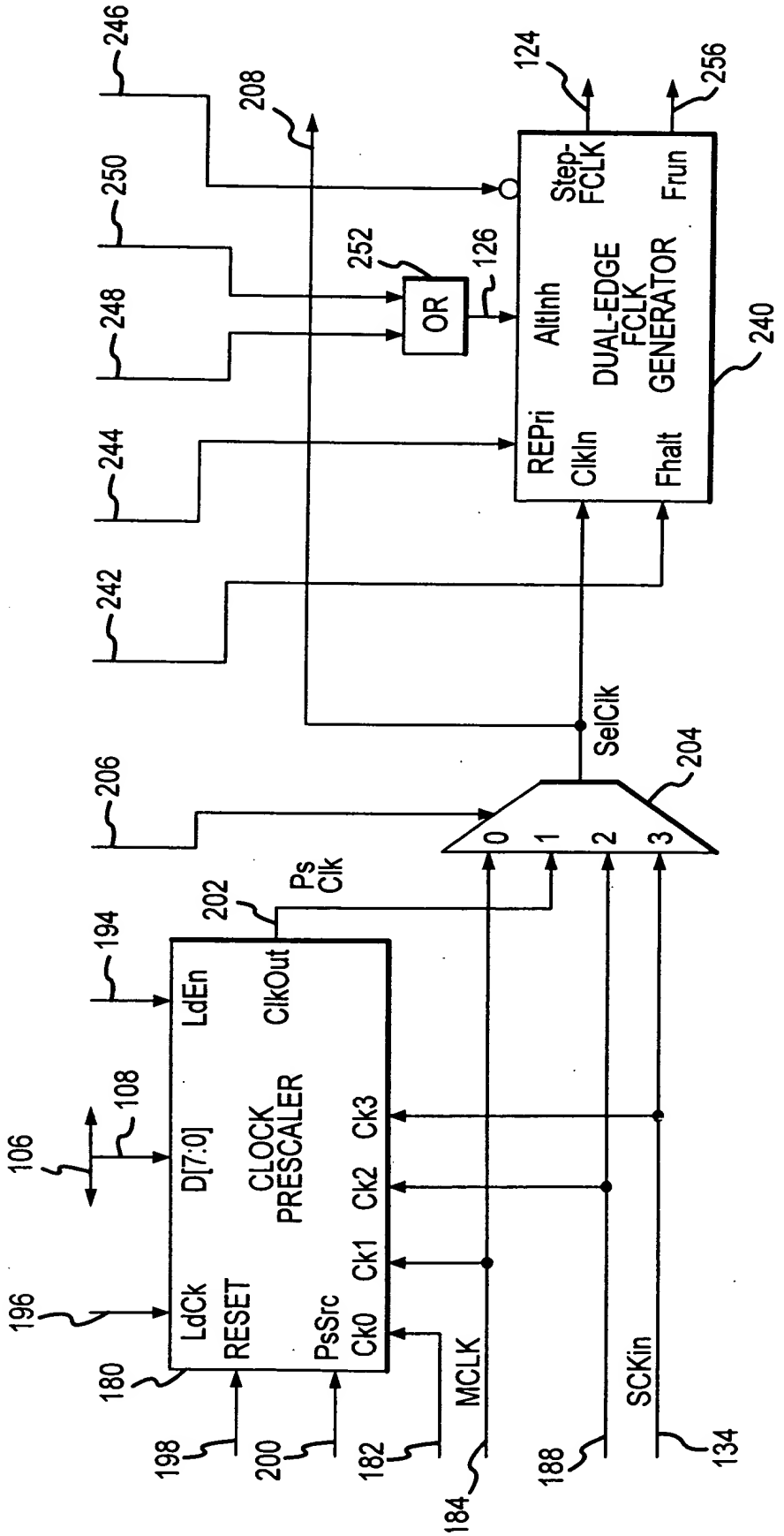

246
208
124
256
250
Step-FCLK
Frun
252
126
248
OR
AltInh
DUAL-EDGE FCLK GENERATOR
240
REPri
ClkIn
Fhalt
244
242
SelClk
204
206
0
1
2
3
Ps Clk
202
194
LdEn
ClkOut
108
106
D[7:0]
CLOCK PRESCALER
Ck3
Ck2
Ck1
Ck0
196
LdCk
RESET
PsSrc
180
198
200
182
MCLK
184
188
SCKin
134

FIG.4

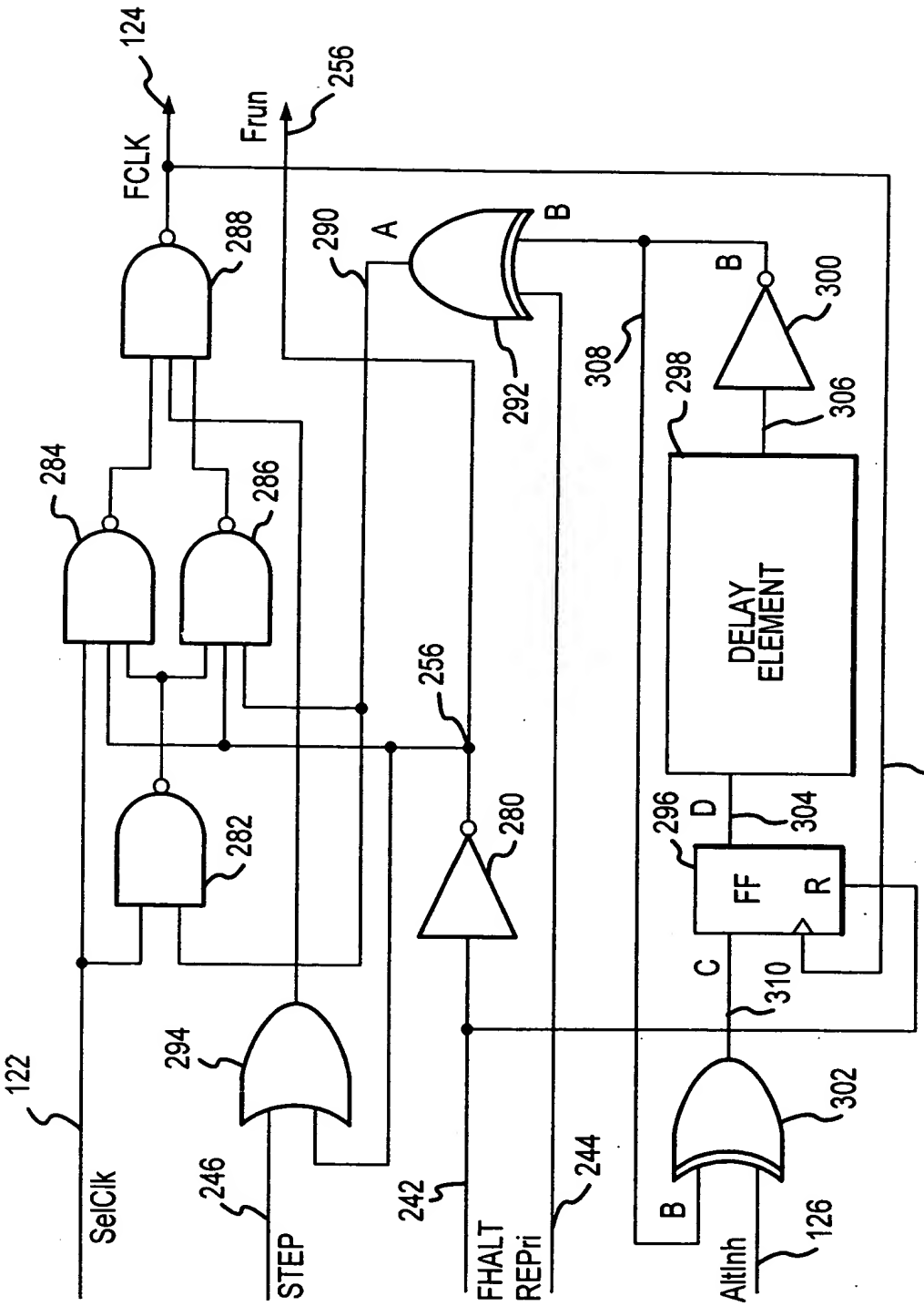

124
FCLK
256
Frun
288
290
A
B
292
308
B
300
298
306
284
286
DELAY
ELEMENT
256
280
282
296
D
304
FF
R
124
C
310
240
294
302
122
SelClk
246
STEP
242
FHALT
REPri
244
B
AltInh
126

FIG.5

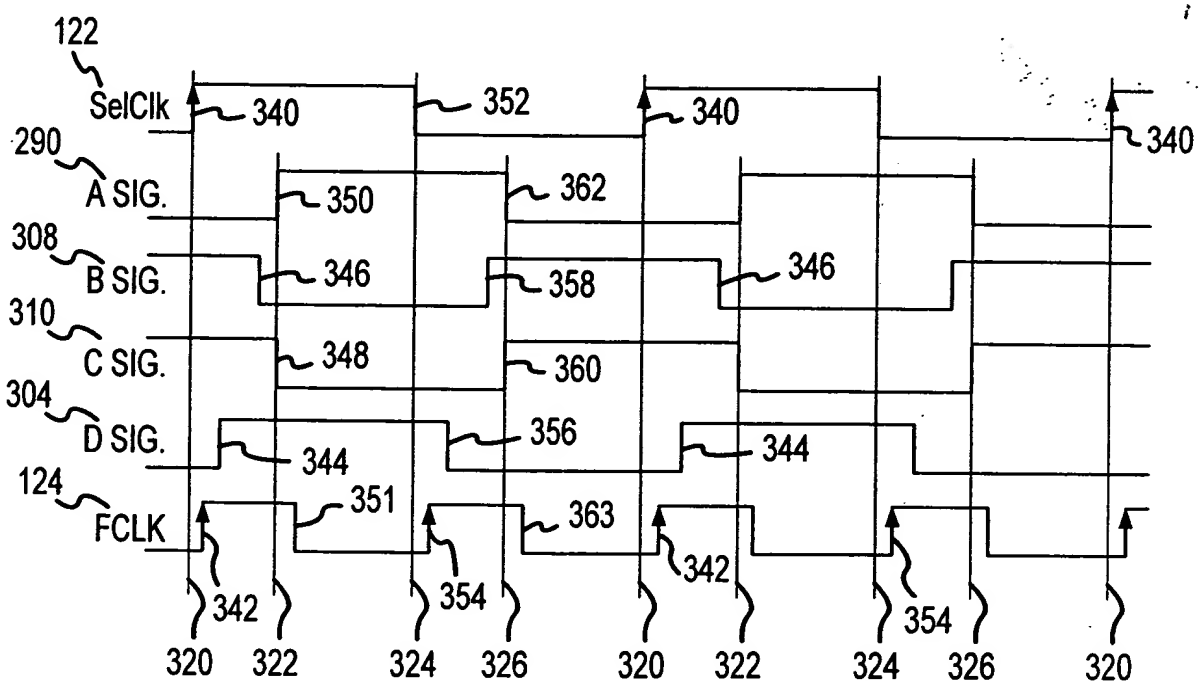

122
SelClk
340
352
340
340
290
A SIG.
350
362
308
B SIG.
346
358
346
310
C SIG.
348
360
304
D SIG.
356
344
344
124
FCLK
351
363
342
342
354
354
320
322
324
326
320
322
324
326
320

FIG.6

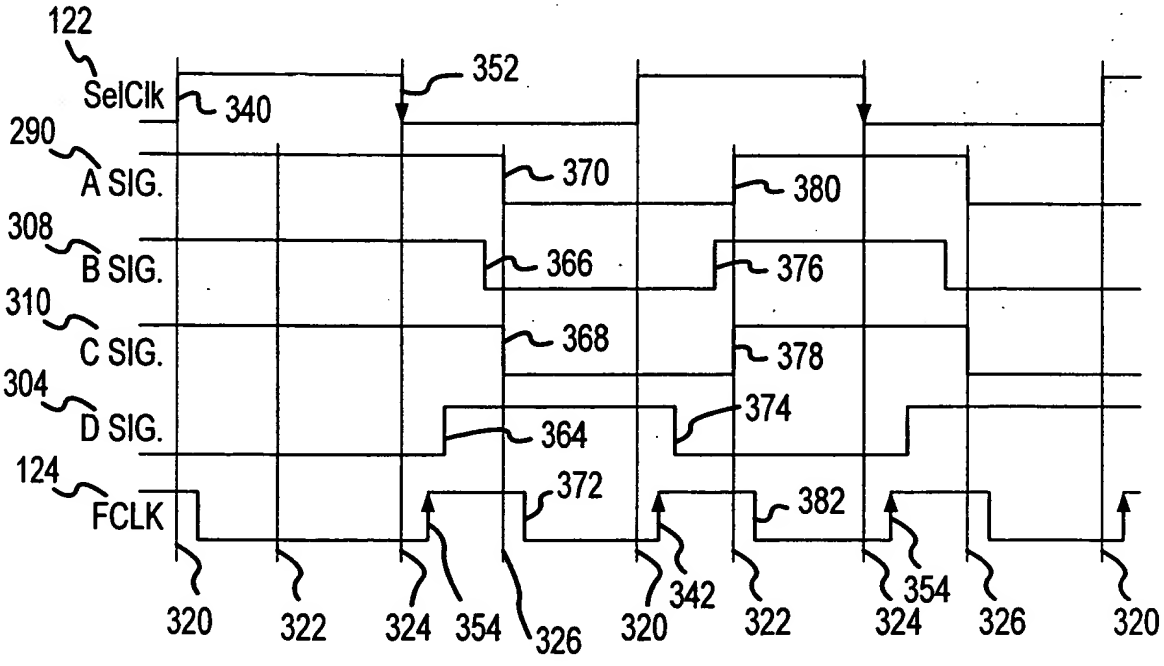

122
SelClk
340
352
290
A SIG.
370
380
308
B SIG.
366
376
310
C SIG.
368
378
304
D SIG.
364
374
124
FCLK
372
382
342
354
320
322
324
354
326
320
322
324
326
320

FIG.7

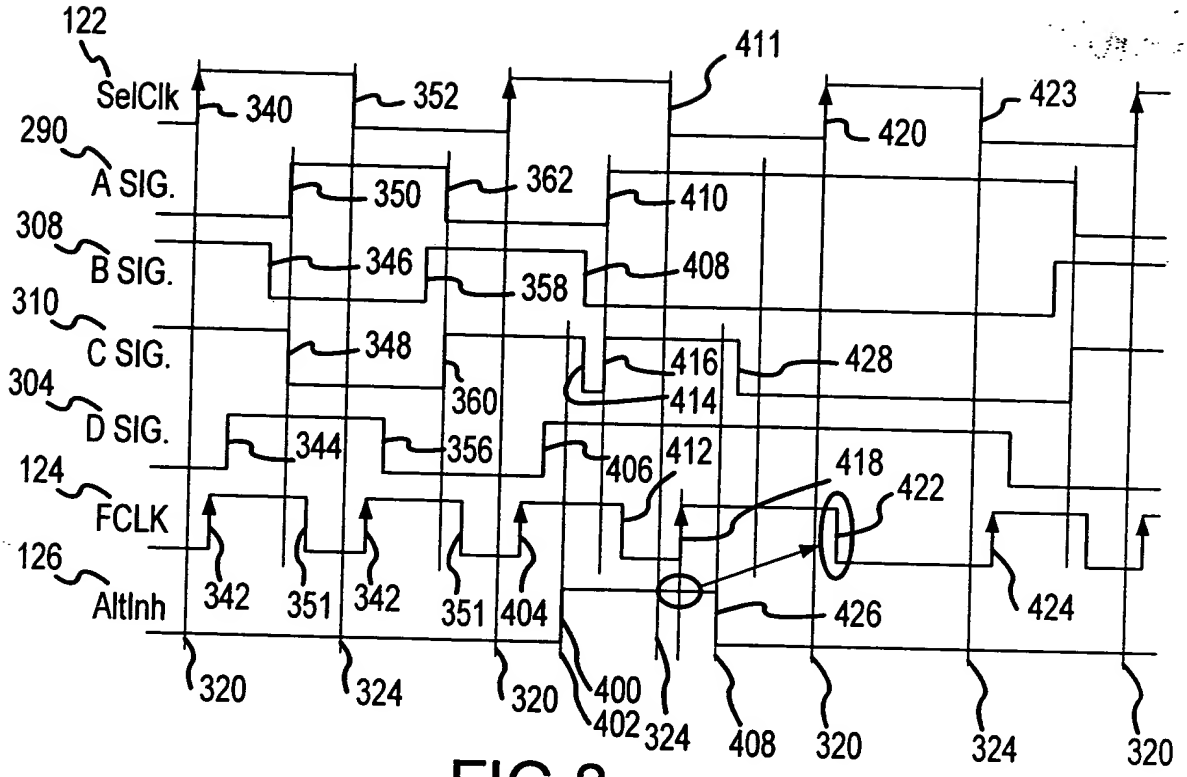

122
SelClk
340
352
411
423
420
290
A SIG.
350
362
410
308
B SIG.
346
358
408
310
C SIG.
348
360
416
428
414
304
D SIG.
344
356
406
412
418
422
124
FCLK
342
351
342
351
404
426
424
126
AltInh
320
324
320
400
402
324
408
320
324
320

FIG.8

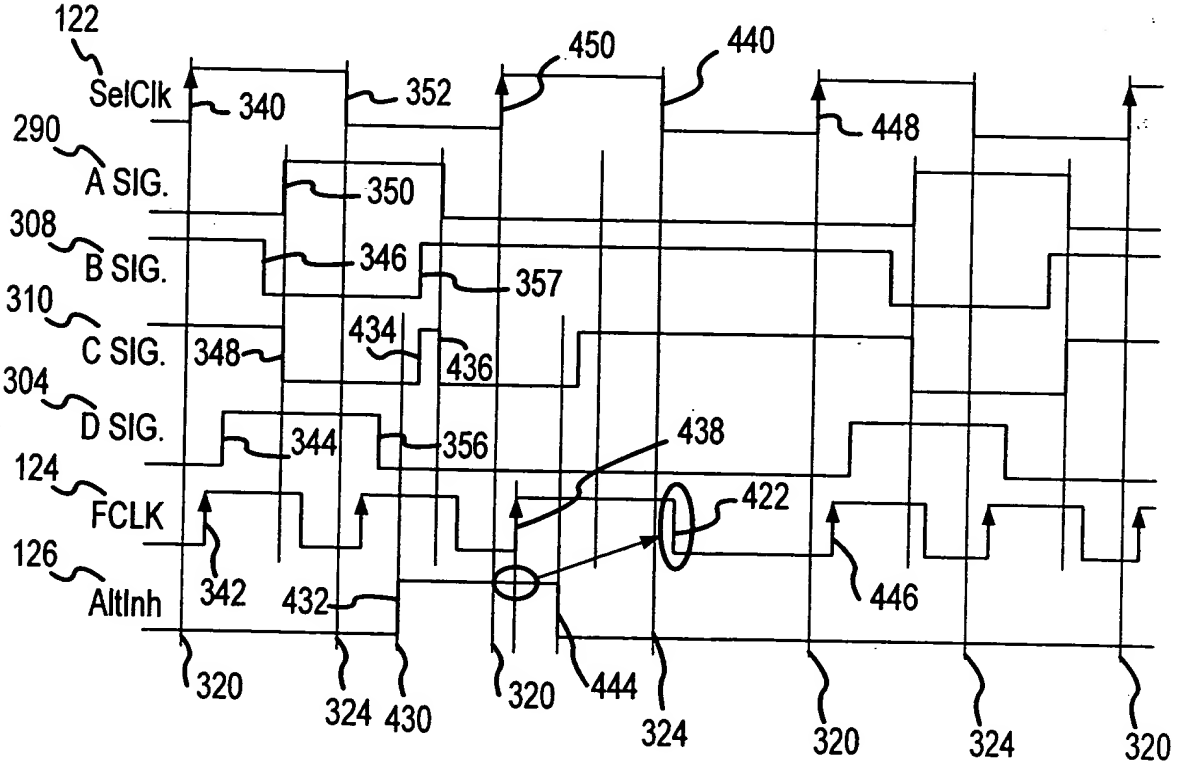

122
SelClk
340
352
450
440
448
290
A SIG.
350
308
B SIG.
346
357
310
C SIG.
348
434
436
304
D SIG.
344
356
438
124
FCLK
422
126
AltInh
342
432
446
320
324
430
320
444
324
320
324
320

FIG.9

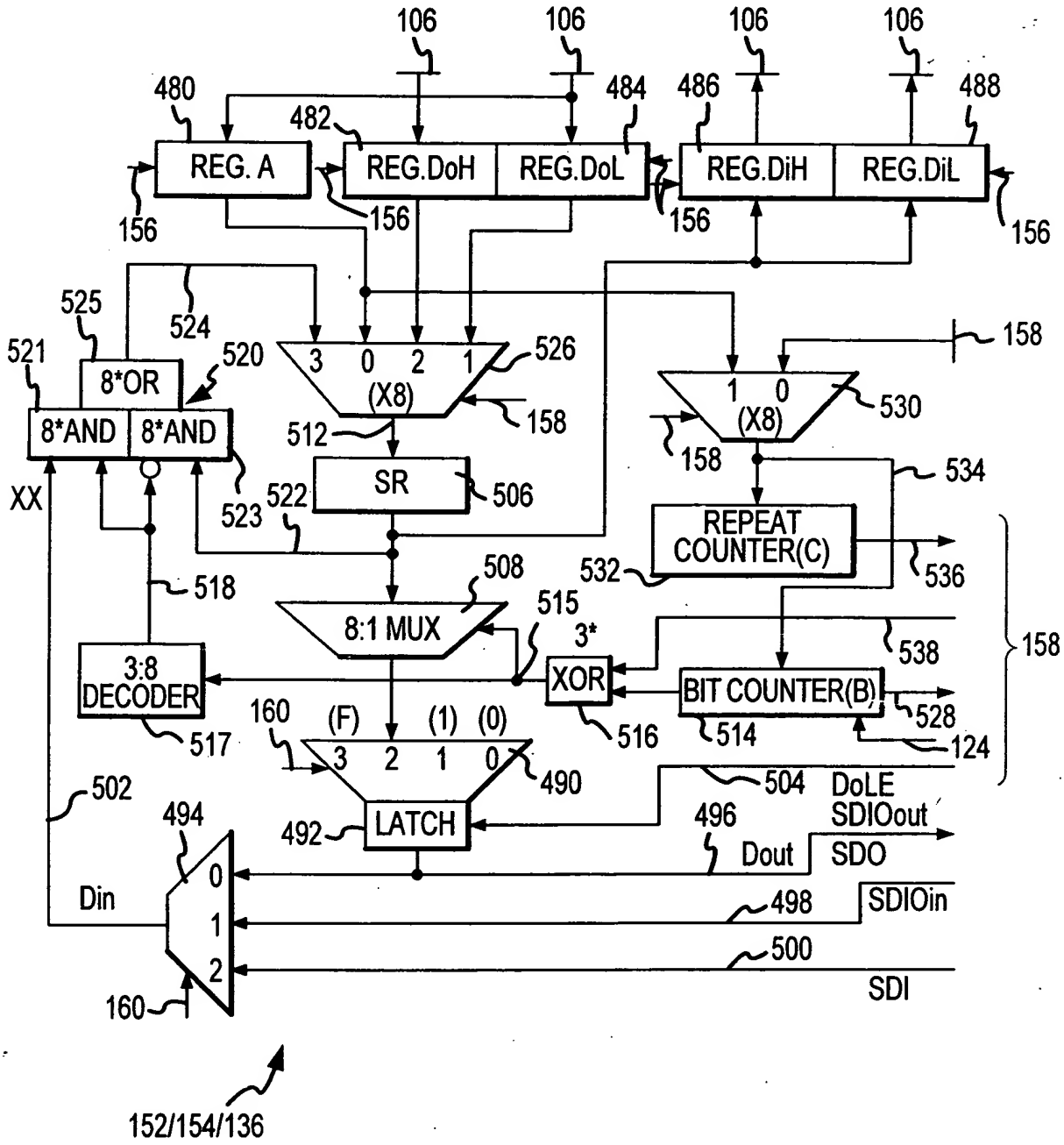

106
106
106
106
480
482
484
486
488
REG. A
REG.DoH
REG.DoL
REG.DiH
REG.DiL
156
156
156
156
525
524
521
520
526
158
8*OR
3 0 2 1
(X8)
1 0
(X8)
530
8*AND
8*AND
512
158
158
534
XX
523
522
SR
506
REPEAT
COUNTER(C)
532
536
518
508
515
8:1 MUX
3*
538
158
3:8
DECODER
XOR
BIT COUNTER(B)
528
517
516
514
124
160
(F)
(1)
(0)
3 2 1 0
490
504
DoLE
502
494
LATCH
492
496
SDIOout
Dout
SDO
Din
0
1
2
498
SDIOin
500
SDI
160
152/154/136

FIG.10

552

INSTRUCTION	7	6	5	4	3	2	1	0
DELAY/NOP	0	0	0	0	0	0	COUNT (C)	

550

0	NOP
1	DELAY 1, SKIP ALT
2	DELAY 2, (USES C)
3	DELAY 3, (USES C)

FIG.11

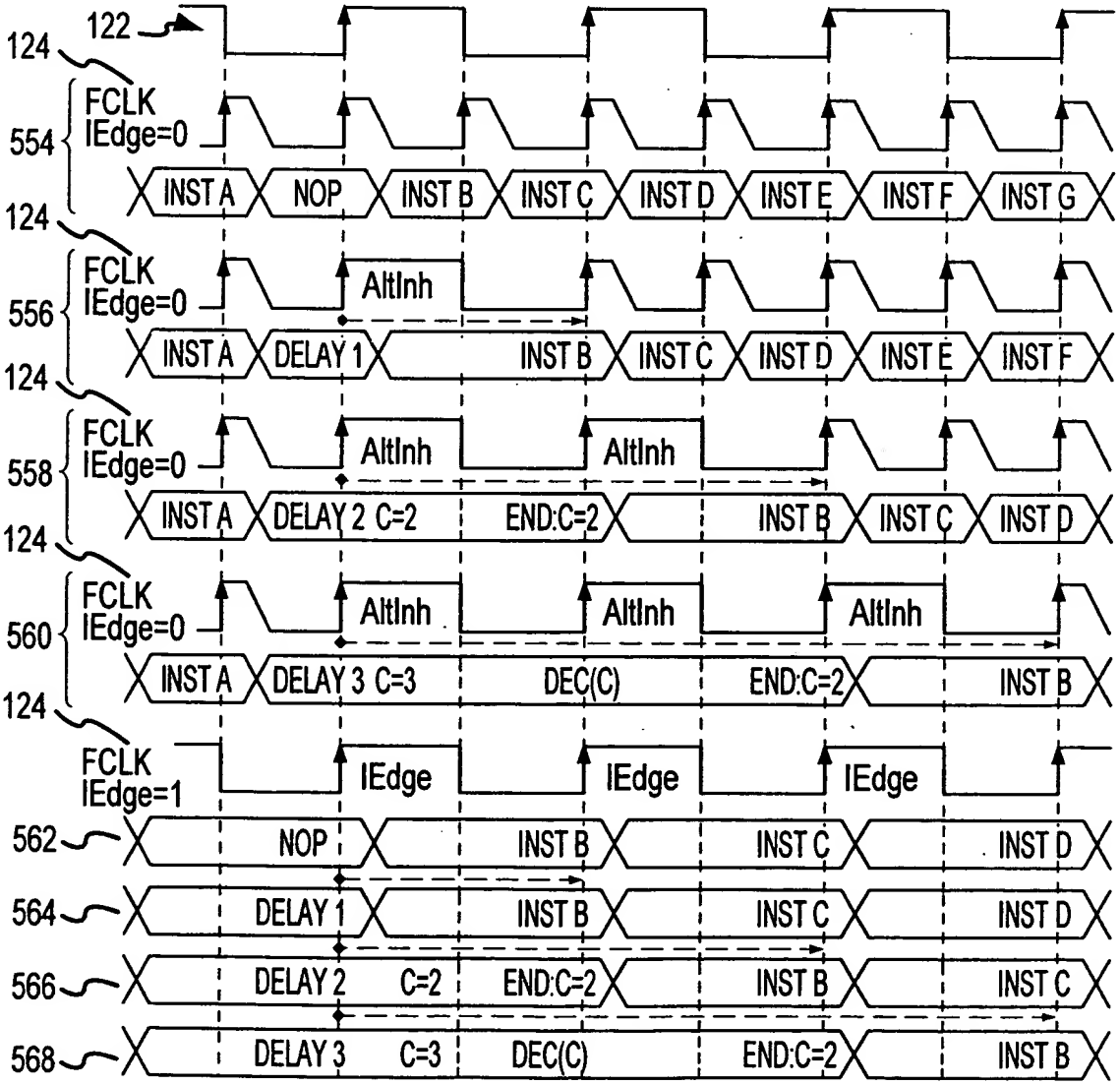


FIG.12

592 594

INSTRUCTION	7	6	5	4	3	2	1	0
WAIT	0	0	0	1	0	0	EVENT	

590

FIG.13

602 604

INSTRUCTION	7	6	5	4	3	2	1	0
OUTnxb	0	0	1	1	0(OUT)	COUNT (C)		
INbnx	0	0	1	1	1(IN)	COUNT (C)		

600

0	RESERVED*
1	OUT/IN, SKIP ALT
2	OUT/IN 2 CYCLES, SKIP ALT
3	OUT/IN 3 CYCLES, SKIP ALT
4	OUT/IN 4 CYCLES, SKIP ALT
5	OUT/IN 5 CYCLES, SKIP ALT
6	OUT/IN 6 CYCLES, SKIP ALT
7	OUT/IN 7 CYCLES, SKIP ALT

FIG.14

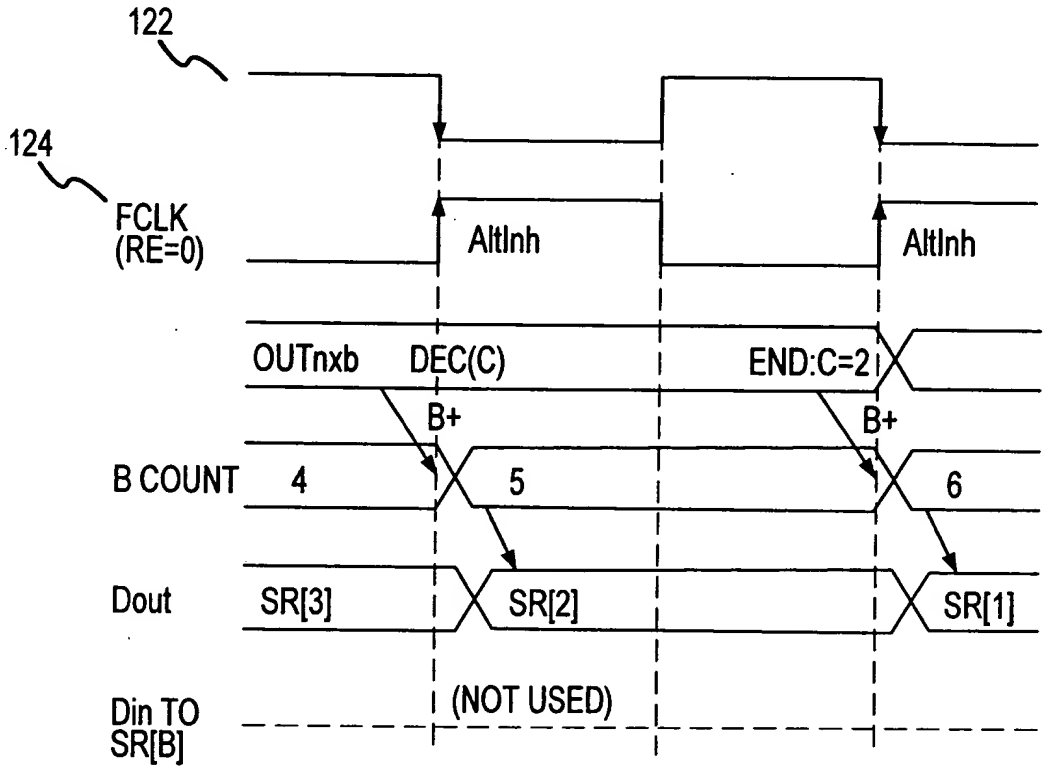

122
124
FCLK
(RE=0)
AltInh
AltInh
OUTnxb
DEC(C)
END:C=2
B+
B+
B COUNT
4
5
6
Dout
SR[3]
SR[2]
SR[1]
Din TO
SR[B]
(NOT USED)

FIG.15

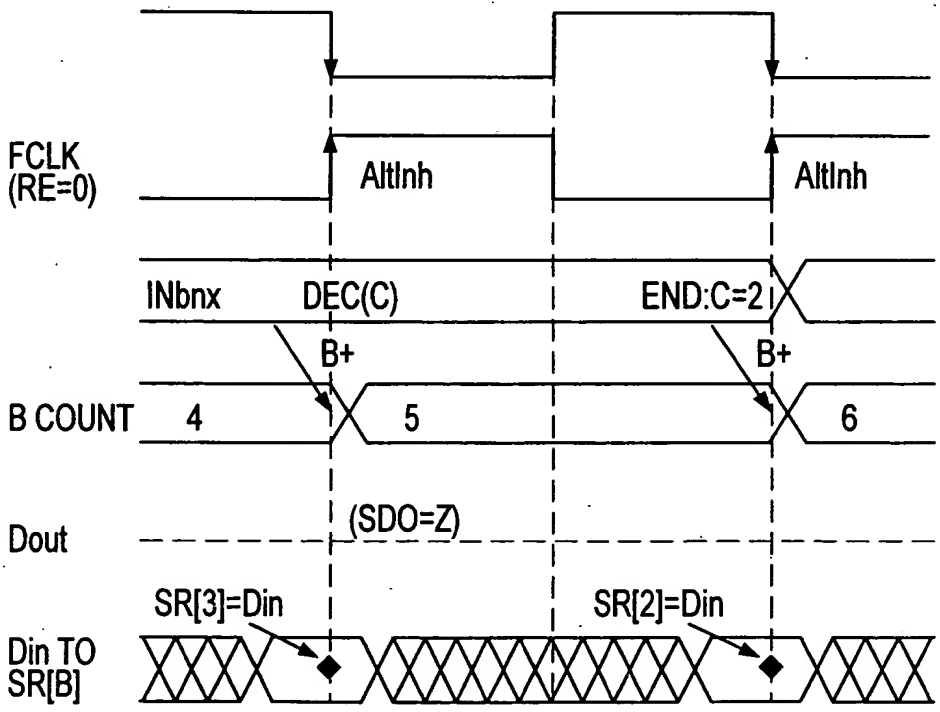

FCLK
(RE=0)
AltInh
AltInh
INbnx
DEC(C)
END:C=2
B+
B+
B COUNT
4
5
6
Dout
(SDO=Z)
SR[3]=Din
SR[2]=Din
Din TO
SR[B]

FIG.16

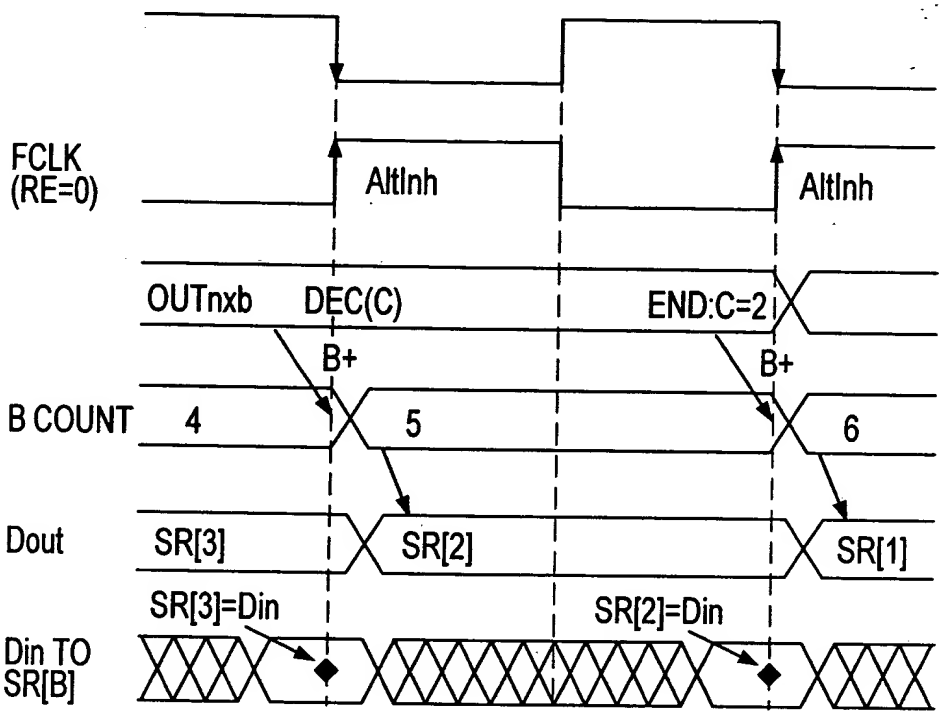

FCLK
(RE=0)
AltInh
AltInh
OUTnxb
DEC(C)
END:C=2
B+
B+
B COUNT
4
5
6
Dout
SR[3]
SR[2]
SR[1]
SR[3]=Din
SR[2]=Din
Din TO
SR[B]

FIG.17

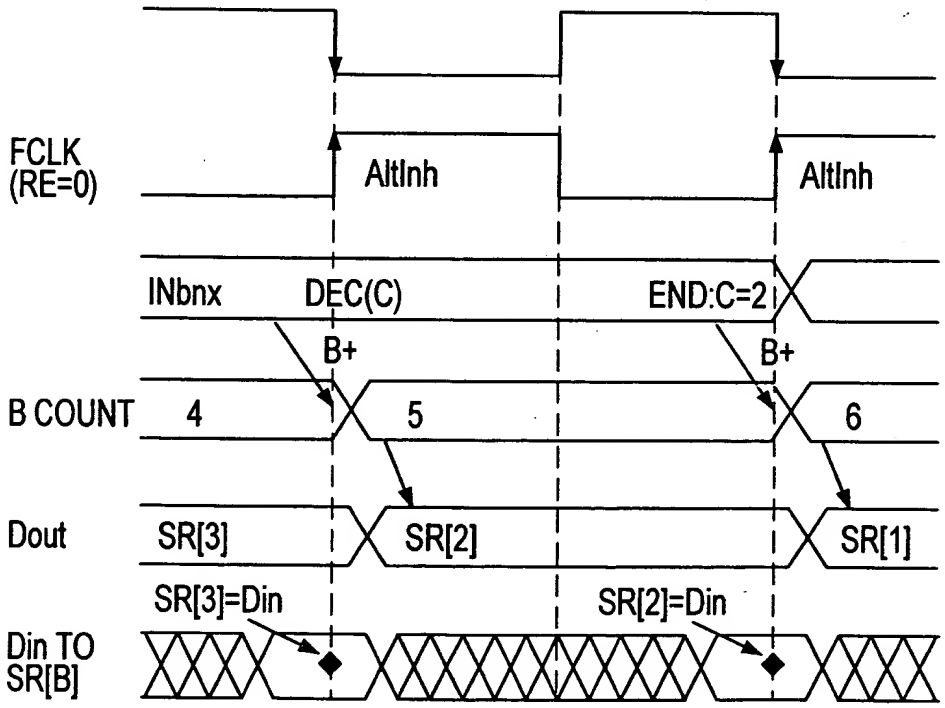

FCLK
(RE=0)
AltInh
AltInh
INbnx
DEC(C)
END:C=2
B+
B+
B COUNT
4
5
6
Dout
SR[3]
SR[2]
SR[1]
SR[3]=Din
SR[2]=Din
Din TO
SR[B]

FIG.18

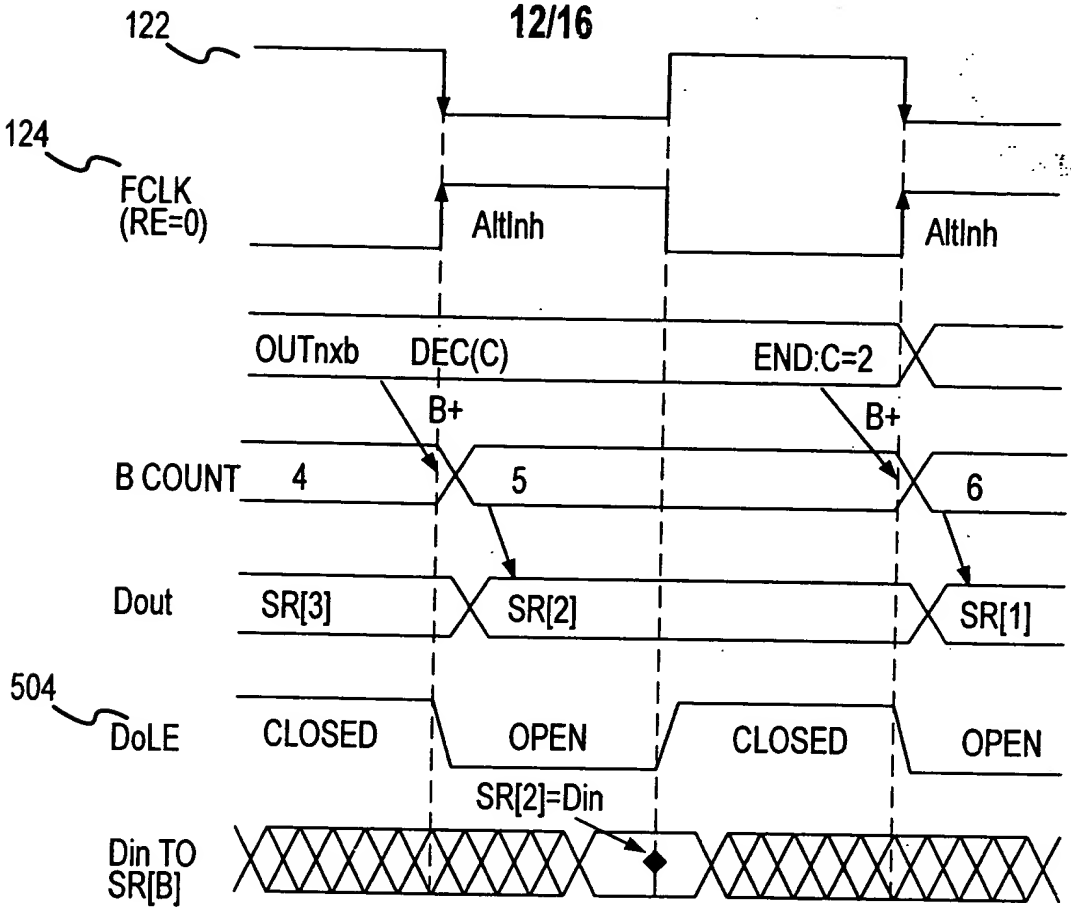
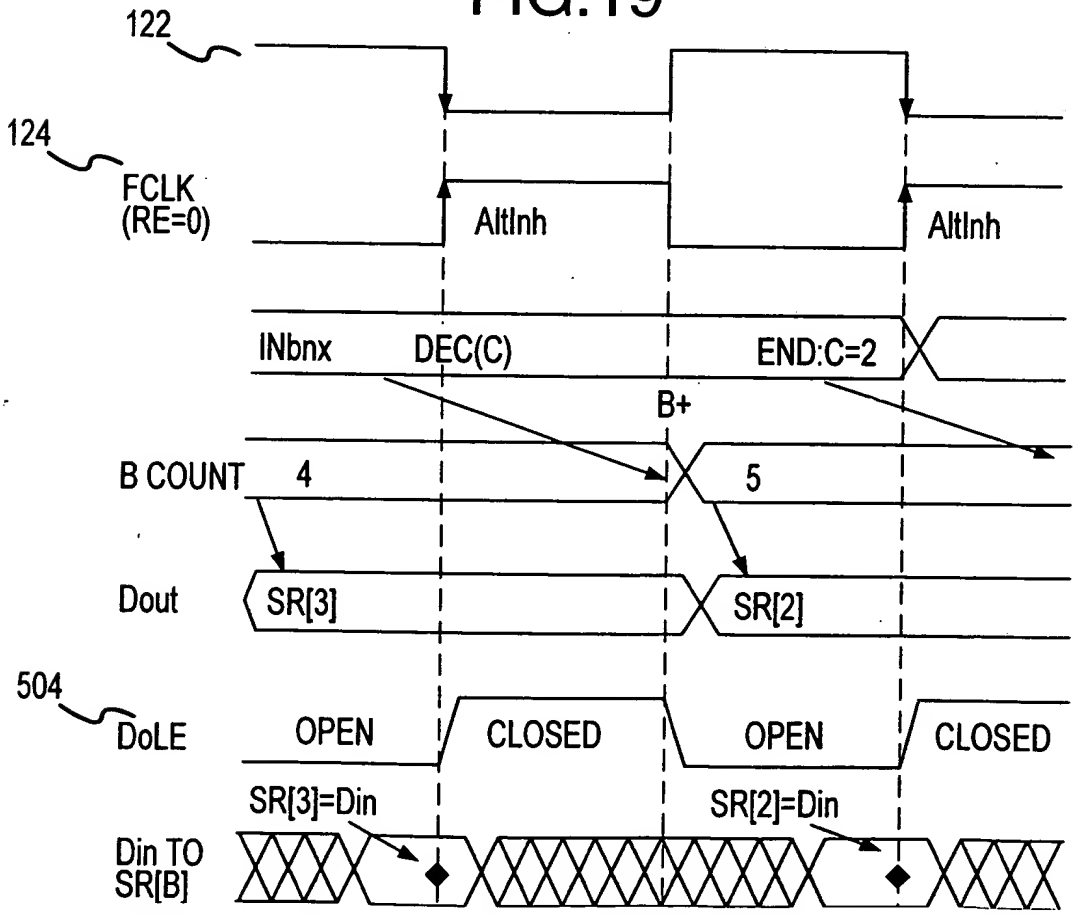

122
124
FCLK
(RE=0)
AltInh
AltInh
OUTnxb
DEC(C)
END:C=2
B+
B+
B COUNT
4
5
6
Dout
SR[3]
SR[2]
SR[1]
504
DoLE
CLOSED
OPEN
CLOSED
OPEN
SR[2]=Din
Din TO
SR[B]

FIG.19


122
124
FCLK
(RE=0)
AltInh
AltInh
INbnx
DEC(C)
END:C=2
B+
B COUNT
4
5
Dout
SR[3]
SR[2]
504
DoLE
OPEN
CLOSED
OPEN
CLOSED
SR[3]=Din
SR[2]=Din
Din TO
SR[B]

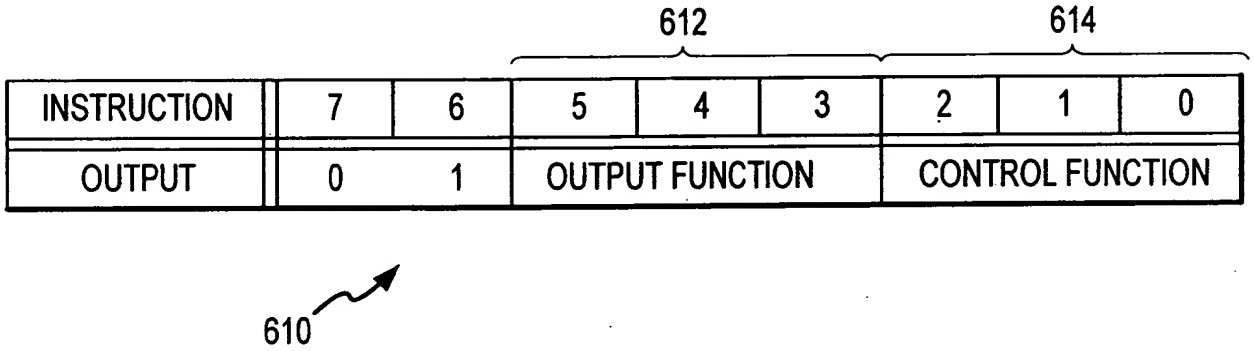

612
614
INSTRUCTION
7
6
5
4
3
2
1
0
OUTPUT
0
1
OUTPUT FUNCTION
CONTROL FUNCTION
610

FIG.21

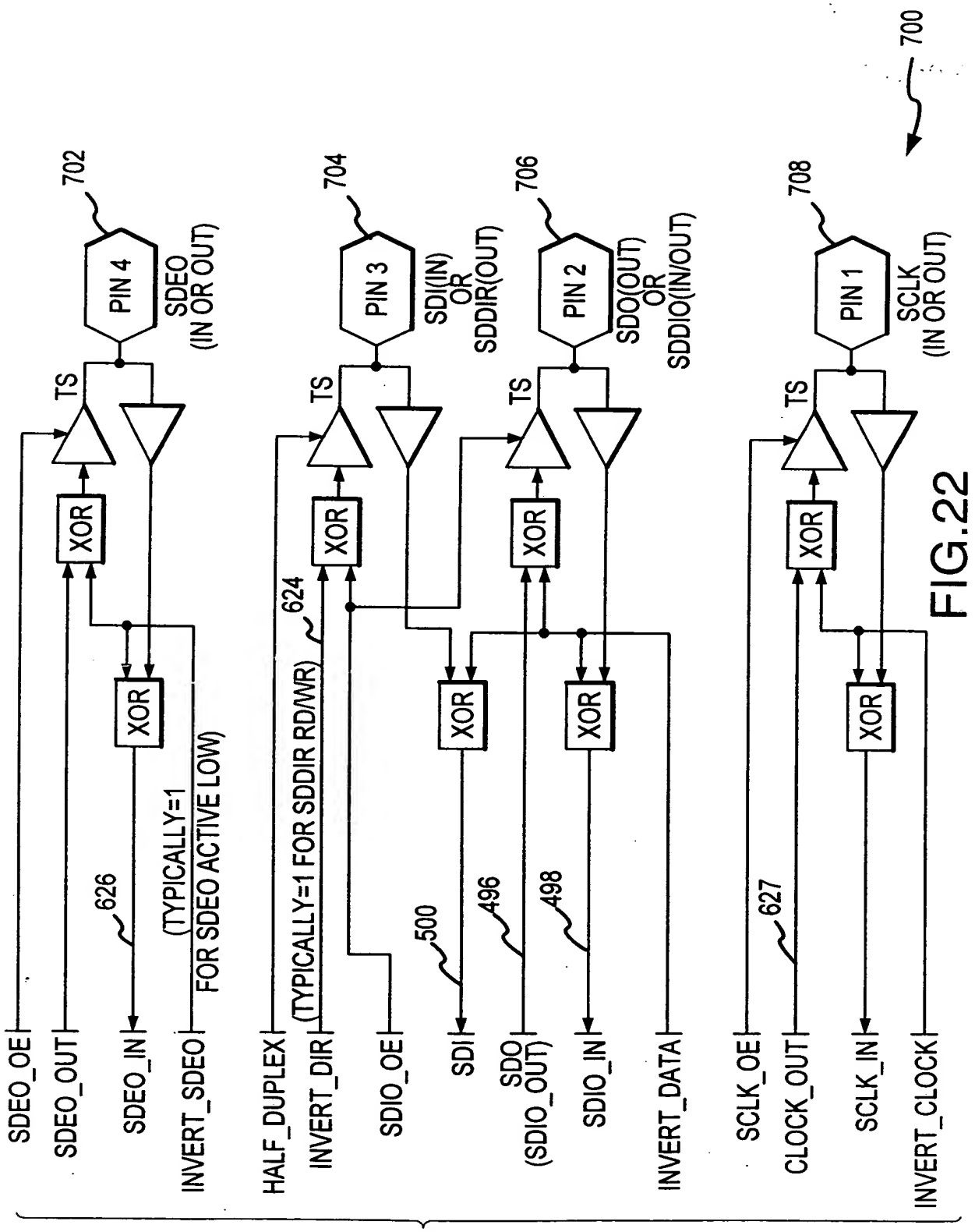

700
702
704
706
708
PIN 4
PIN 3
PIN 2
PIN 1
SDEO (IN OR OUT)
SDI(IN) OR SDDIR(OUT)
SDO(OUT) OR SDDIO(IN/OUT)
SCLK (IN OR OUT)
TS
XOR
SDEO_OE
SDEO_OUT
SDEO_IN
INVERT_SDEO
(TYPICALLY=1 FOR SDEO ACTIVE LOW)
626
HALF_DUPLEX
INVERT_DIR
(TYPICALLY=1 FOR SDDIR RD/WR)
624
SDIO_OE
SDI
SDO (SDIO_OUT)
SDIO_IN
INVERT_DATA
500
496
498
SCLK_OE
CLOCK_OUT
SCLK_IN
INVERT_CLOCK
627
138

FIG.22

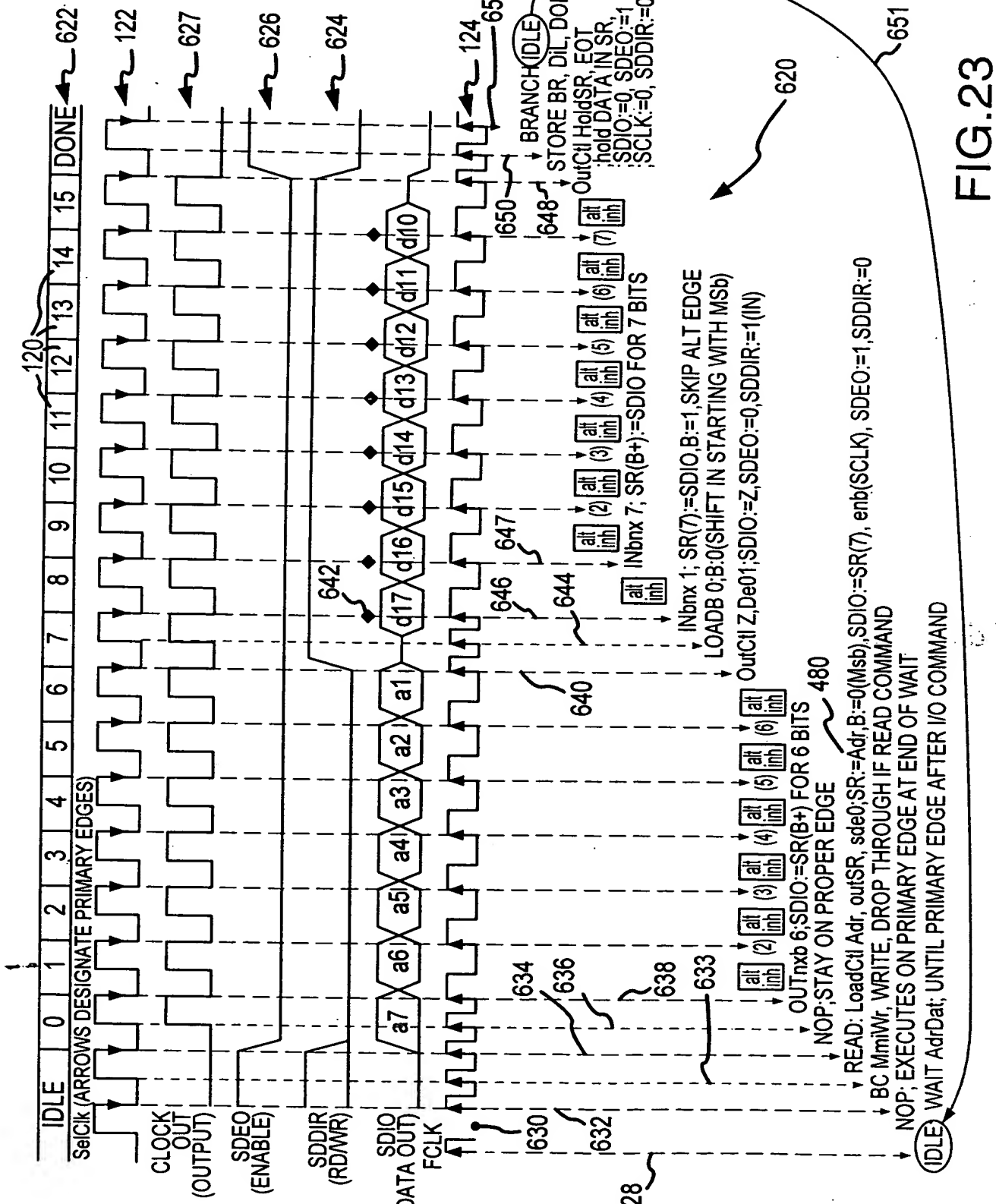

IDLE
SelClk (ARROWS DESIGNATE PRIMARY EDGES)
CLOCK OUT (OUTPUT)
SDEO (ENABLE)
SDDIR (RD/WR)
SDIO (DATA OUT)
FCLK
DONE
120
122
124
622
624
626
627
628
630
632
633
634
636
638
640
642
644
646
647
648
650
651
652
620
480
a7 a6 a5 a4 a3 a2 a1 d17 d16 d15 d14 d13 d12 d11 d10
alt inh
OUTnxb 6;SDIO:=SR(B+) FOR 6 BITS
NOP;STAY ON PROPER EDGE
READ: LoadCtl Adr, outSR, sde0;SR:=Adr,B:=0(Msb),SDIO:=SR(7), enb(SCLK), SDEO:=1,SDDIR:=0
BC MmiWr, WRITE, DROP THROUGH IF READ COMMAND
NOP; EXECUTES ON PRIMARY EDGE AT END OF WAIT
WAIT AdrDat; UNTIL PRIMARY EDGE AFTER I/O COMMAND
OutCtl Z,De01;SDIO:=Z,SDEO:=0,SDDIR:=1(IN)
INbnx 1; SR(7):=SDIO,B:=1,SKIP ALT EDGE
LOADB 0;B:0(SHIFT IN STARTING WITH MSb)
INbnx 7; SR(B+):=SDIO FOR 7 BITS
STORE BR, DIL, DONE
BRANCH (IDLE)
OutCtl HoldSR, EOT
;hold DATA IN SR,
;SDIO:=0, SDEO:=1
;SCLK:=0, SDDIR:=0

FIG.23

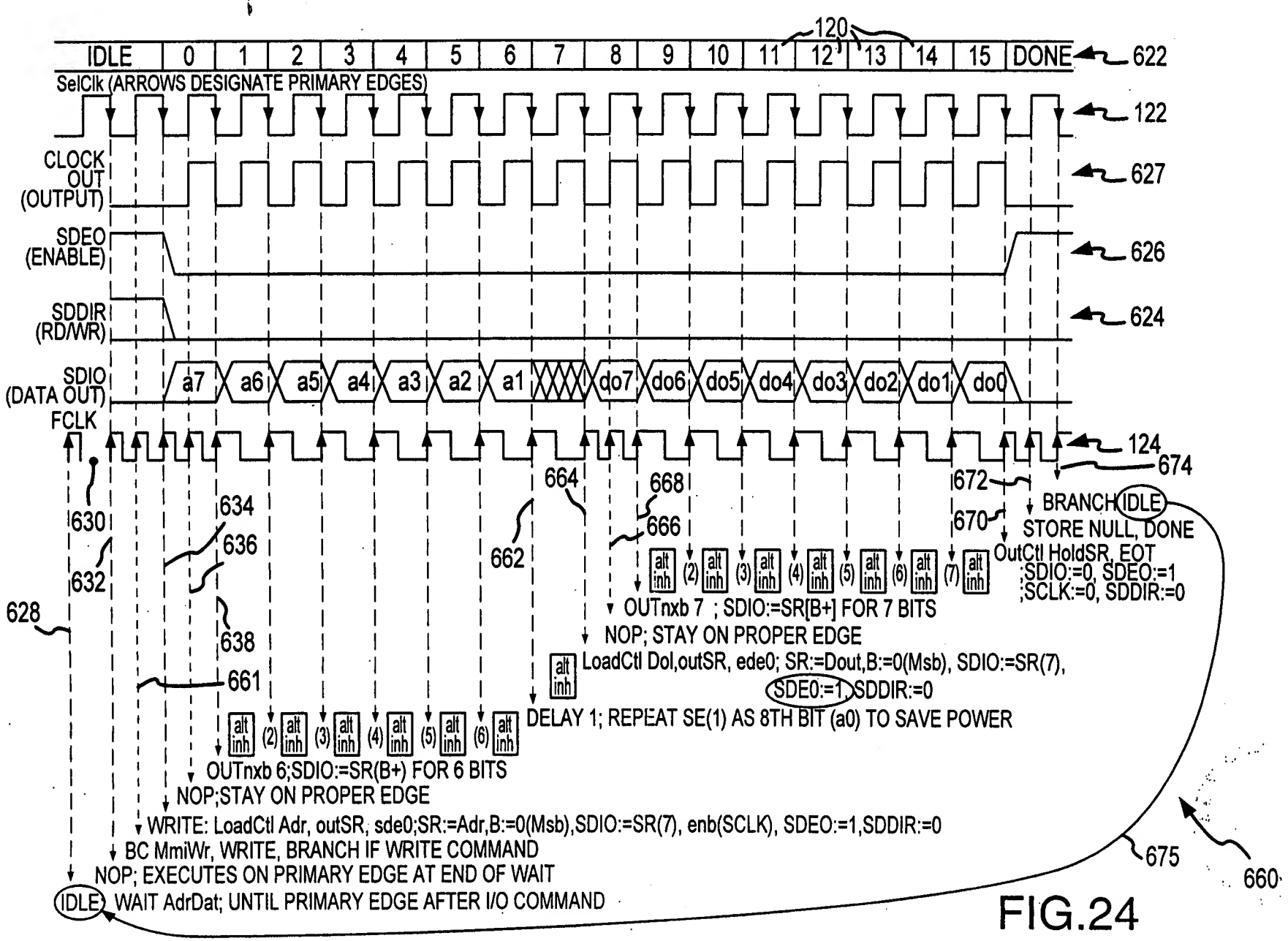

120
IDLE
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
DONE
622
SelClk (ARROWS DESIGNATE PRIMARY EDGES)
122
CLOCK OUT (OUTPUT)
627
SDEO (ENABLE)
626
SDDIR (RD/WR)
624
SDIO (DATA OUT)
a7
a6
a5
a4
a3
a2
a1
do7
do6
do5
do4
do3
do2
do1
do0
FCLK
124
674
672
664
668
666
662
630
634
636
632
670
BRANCH IDLE
STORE NULL, DONE
OutCtl HoldSR, EOT
;SDIO:=0, SDEO:=1
;SCLK:=0, SDDIR:=0
alt inh
(2)
(3)
(4)
(5)
(6)
(7)
OUTnxb 7 ; SDIO:=SR[B+] FOR 7 BITS
NOP; STAY ON PROPER EDGE
628
638
LoadCtl Dol,outSR, ede0; SR:=Dout,B:=0(Msb), SDIO:=SR(7),
SDE0:=1 SDDIR:=0
661
DELAY 1; REPEAT SE(1) AS 8TH BIT (a0) TO SAVE POWER
OUTnxb 6;SDIO:=SR(B+) FOR 6 BITS
NOP;STAY ON PROPER EDGE
WRITE: LoadCtl Adr, outSR, sde0;SR:=Adr,B:=0(Msb),SDIO:=SR(7), enb(SCLK), SDEO:=1,SDDIR:=0
BC MmiWr, WRITE, BRANCH IF WRITE COMMAND
NOP; EXECUTES ON PRIMARY EDGE AT END OF WAIT
IDLE
WAIT AdrDat; UNTIL PRIMARY EDGE AFTER I/O COMMAND
675
660

FIG.24